AN1294 APPLICATION NOTE

PowerSO-10RF: THE FIRST TRUE RF POWER SMD PACKAGE

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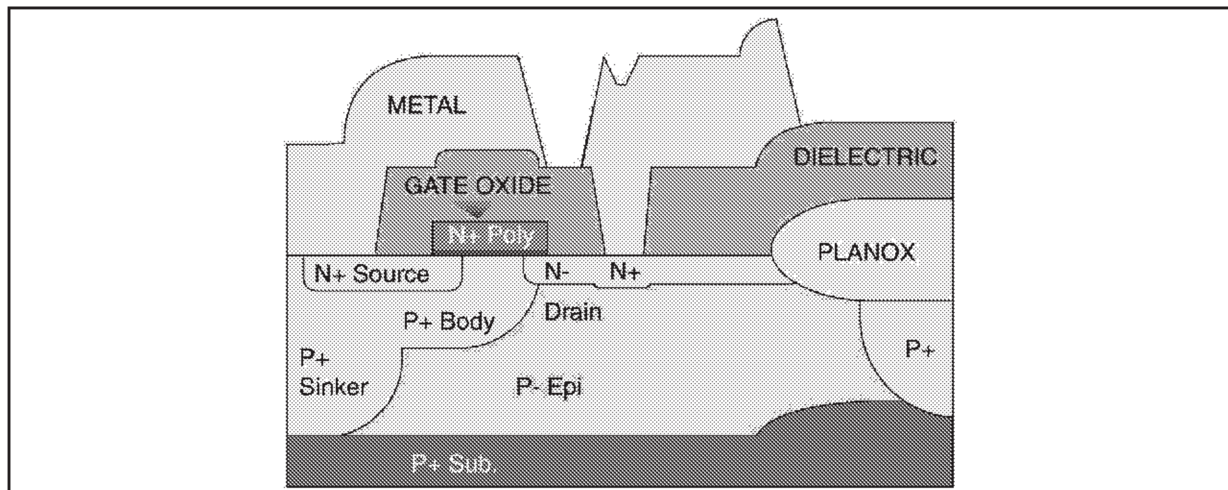
1. ABSTRACT

During the last 10 years, as the size of electronic assemblies decreased and their reliability increased, there has been a need across the board for various components which have to be surface mounted. PowerSO-10RF is not just a new package, it is a new concept in a small outline plastic package for RF power applications. In such applications there is a great need for Surface Mount (SMD) packages but, up until now, the available bipolar technology did not allow it. The main advantages of this new RF plastic package are excellent thermal performance, high power capability, high power density and suitability for all reflow soldering methods. This application note will show that the PowerSO-10RF is the perfect solution for the new RF power LDMOS products recently introduced by STMicroelectronics.

2. POWER RF PACKAGE REQUIREMENTS.

The most important requirement in a power RF package is good heat dissipation capability. The package must be able to dissipate heat so that die temperature remains below a pre-definite maximum temperature above which damage might occur. Other important features of a good RF package are: low inter-electrode capacitance, low parasitic inductance, high electrical conductivity, reliability and low cost.

Figure 1: LDMOS Structure



In DMOS or Bipolar conventional vertical technology, an electrical insulator (Beryllium oxide: BeO which is highly toxic) is required to isolate the drain from the ground. In a LDMOS structure where both the N+ source and the drain region are on the die surface with a laterally diffused low resistance P+ sinker connecting the source region to the P+ substrate and source terminal (see figure 1), this insulator is no longer needed, this not only means that electrical and thermal performances are greatly improved but also

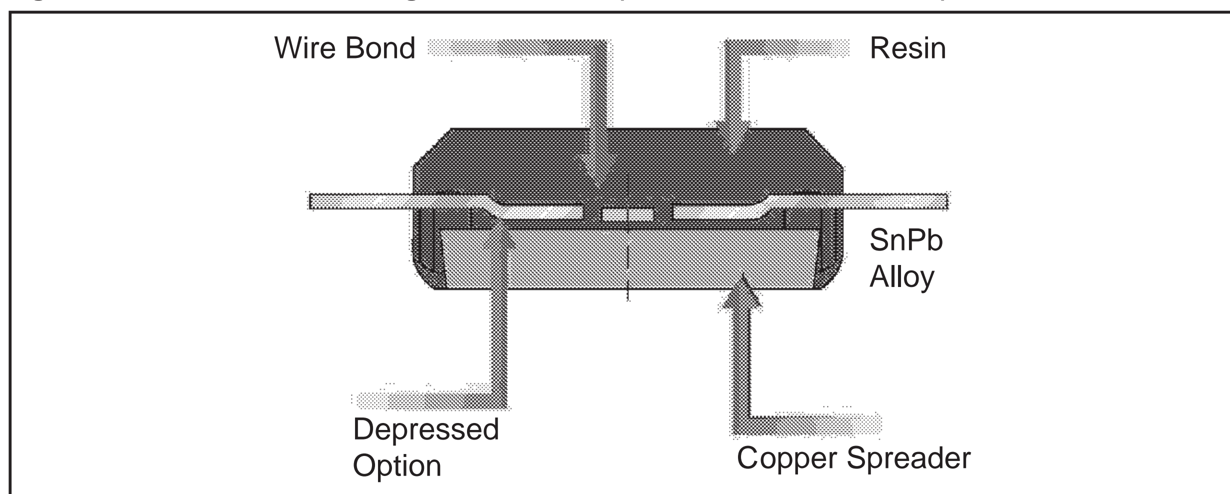
that the standard DMOS ceramic package (with BeO) used for 1W and above devices can be replaced by a plastic package.

3. WHAT IS PowerSO-10RF?

PowerSO-10RF is an RF optimized version of PowerSO-10™. It is the first ST JEDEC approved high power SMD package and already in production for almost 10 years, mainly for products such as rectifiers, protection diodes, triacs, power transistors (Bipolar, MOSFETs & IGBTs), which have already proven their reliability in Automotive, Telecom & Computer applications where reliability standards are very high.

3.1 Brief Overview of PowerSO-10RF technology.

Figure 2: PowerSO-10RF Package Construction (JEDEC MO-184 Standard)



The plastic package of a power chip has four main functions:

- Electrical interconnection between the silicon LDMOS chip and the external circuit;
- Protection from chemically aggressive agents, for long-term reliability;
- Mechanical support to the LDMOS die to make handling easier;
- A thermally conductive path to transfer the heat generated in operation from the silicon LDMOS die to the ambient or to the heatsink.

PowerSO-10RF is the result of an optimization between conflicting requirements of good thermal properties and small dimensions. Its low thermal resistance is a result of a large copper heat spreader (slug) integrated into the package body, in direct contact with the silicon LDMOS die.

The metal ”chassis” of the device, consisting of the copper slug (Cu/KFC) and the package leads is known as the leadframe (Cu/CUPROFOR). The leadframes for a number of individual devices are manufactured in a single continuous strip to simplify handling and processing.

After the silicon LDMOS wafer is cut into individual dice, the die are brazed onto the copper slug using a high melting temperature (>280°C) tin solder alloy such as Pb97.5Sn1Ag1.5.

The process used to attach die to the slug is critical to maintain the thermal performance of the RF power device. It must produce a uniform, voids free joint between the silicon LDMOS back metallization and the copper slug, in order to avoid hot spots in the active area and, in long terms, through thermal fatigue.

After the die is attached, the silicon LDMOS die is connected to the lead-frame with Au or Al wires which are ultrasonically bonded to both the metallization on the chip (Al alloy: AlSiCu) and to a nickel layer on the leadframe. The diameter of the wire used is chosen according to the current to be handled using the approximated rule of about 1mil (25 µm) per Amp.

Molding is the third step of assembly; the leadframe strips are positioned in molding cavities, which are then pressure filled with liquid thermosetting epoxy; which after solidification provides a hard, reliable and cost effective encapsulation. (Molding compound: Sumitomo Eme 6300HV with a molding temperature of 200°C +/- 20°C).

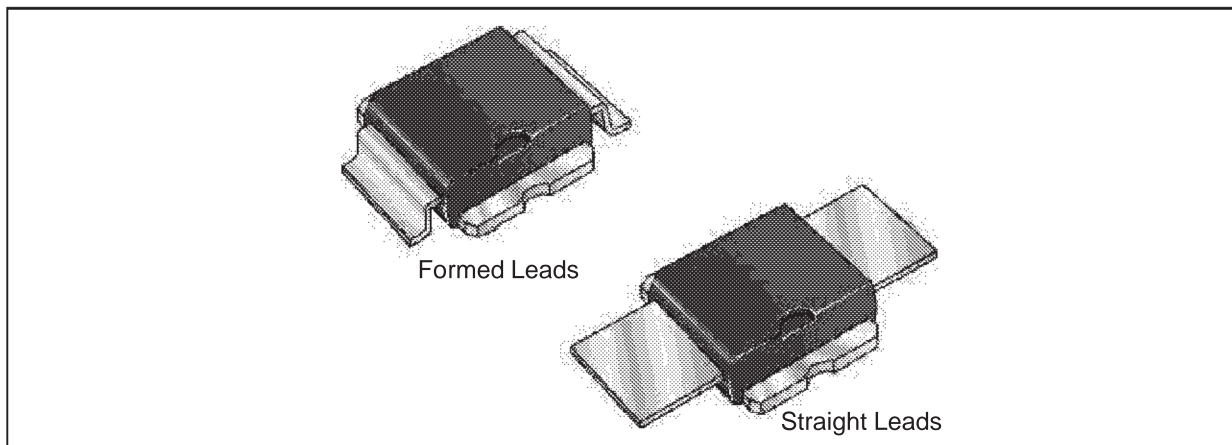
The last major process is to coat the leads with a low melting temperature thin solder alloy (tin plating: 7µm min / 15µm max) to provide a ”wettable” surface when the device is soldered to the printed circuit board (PCB).

After singulation (separation of the leadframe strips into individual devices) and lead forming (bending of the leads into the required shape), devices are marked and tested before being packed and shipped.

Note: There are two available lead versions (see figure 3):

- Formed leads for SMD applications and power dissipation (Pdiss.) < 15W
- Straight leads for standard RF mounting on heatsink and Pdiss. > 15W

Figure 3: PowerSO-10RF Straight and Formed Lead Versions



Delivery information:

- Tube of 50 pieces / Bulk quantity = 250 pieces (available for both lead versions)
- Tape & Reel of 600 pieces

4. PRODUCTS.

The PowerSO-10RF LDMOS products family (PDxxxxx series) allies the high linearity and improved thermal performances of ST's cutting edge LDMOS technology to the low cost, high performance advantages of plastic packages. It is a perfect solution for high volume portable, mobile and base station applications for which space and cost are essential factors.

4.1 BENEFITS.

- Balanced weight;
- Good Coplanarity;
- Reliable solder joint;
- Good heat conduction;
- Junction Temperature 165°C;
- Max power dissipation. 150W;
- Improved RF performances (Operation >1GHz).

Table 1: PowerSO-10RF features and benefits

Designed with…	**To the package & product**…	**To the customer**…
Large heat conductive slug	Excellent thermal performance	True RF high power SMD products for pick & place assembly
Good solderability	Balanced weight + excellent lead coplanarity for optimal leads & slug contact with PCB + solder reflow quality inspection points	Simple automatic assembly + high reliability + easy quality control + compatible with industry standard mounting techniques
Careful choice of materials + consideration of hermetic properties	JEDEC standard	Peace of mind + simple sourcing + high component reliability
Compact dimensions coupled with high current capability	Ability to withstand high junction temperature + extended operating temperature range	Product ideally suited to adverse environment
Leadframe designed for low parasitic inductance	Improved RF performances	RF broadband capability

4.2 SEGMENTS AND APPLICATIONS.

- Military Communications (HF/VHF)
- VHF-UHF Analog & Digital PMR (Portable, Mobile & BTS)
- TV Band IV-V (470-860 MHz)
- Cellular BTS: IS-36, IS-54, IS-95, GSM900, GSM1800, PCS1900, W-CDMA etc.

5. LDMOS in PowerSO-10RF / TYPICAL RF PERFORMANCES.

LDMOS transistors are today used successfully in several digital applications such as cellular base station, HDTV, TETRA etc. and have already proven their advantages versus bipolar transistors such as:
- Higher power gain;
- Input impedance more constant under varying drive levels;
- Better IMD performances;
- Easier to bias;
- Gain control by varying the DC gate bias voltage;
- Better thermal behavior;
- Less overall system cost.

Moreover, LDMOS products in PowerSO-10RF display similar or better performances than its equivalent in ceramic package such as power gain (similar) and thermal resistance (~10% lower):

Figure 4: PD57045S in PowerSO-10RF versus SD57045-01 in Ceramic

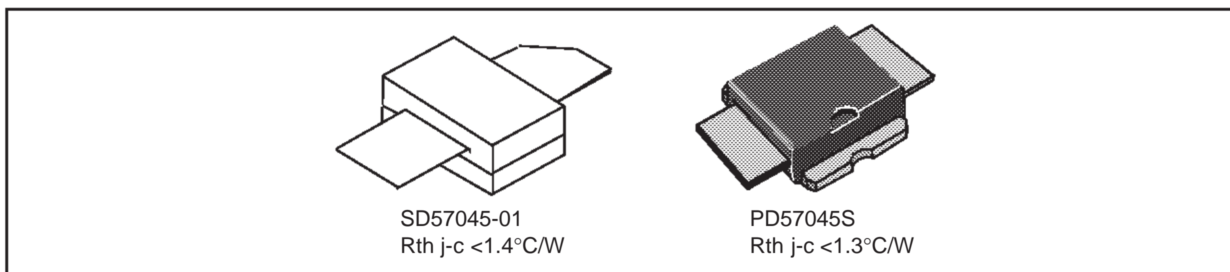
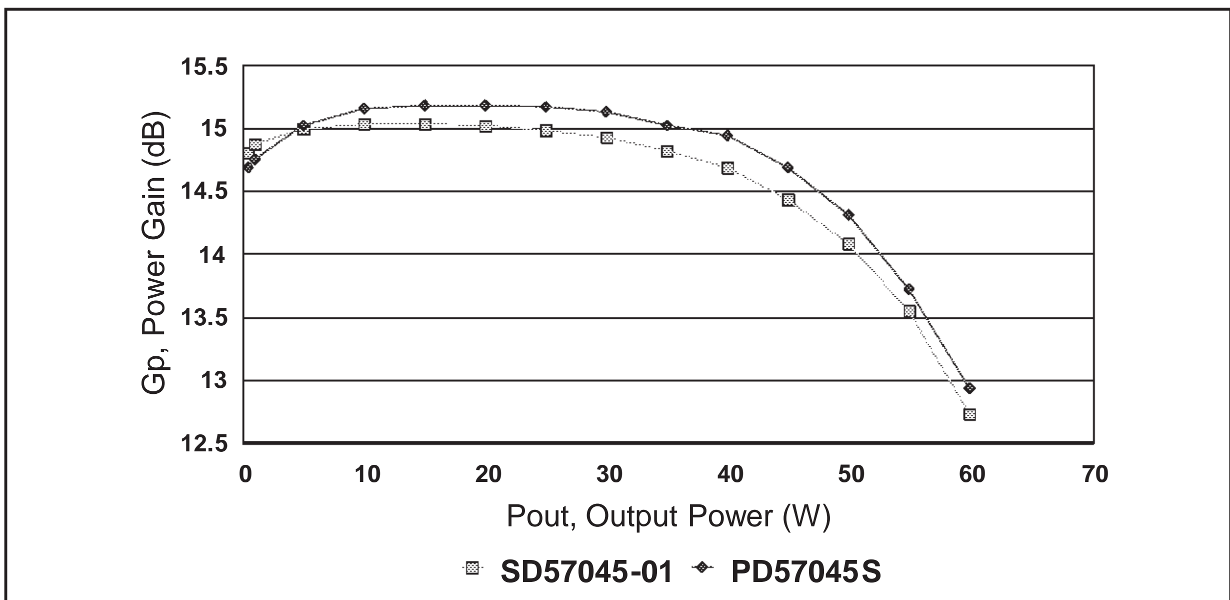


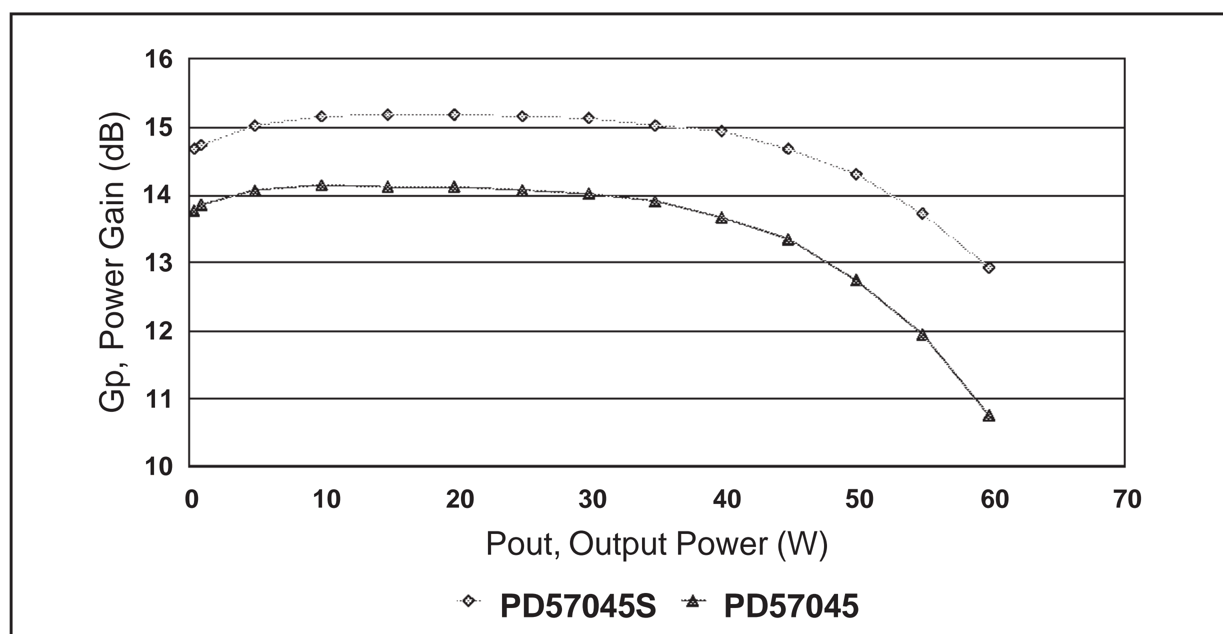
Figure 5: Power gain versus Output power / Ceramic vs. Plastic



Note:

LDMOS products in PowerSO-10RF straight leads display slightly better RF power gain (up to +1.5dB) than the same products in PowerSO-10RF formed leads. This is mainly due to the parasitic reactance induced by the physical lead shape. However, this slight loss in gain is greatly overcome by the SMD capability advantages of PowerSO-10RF formed leads version.

Figure 6: Power gain versus output power / Straight leads vs. Formed leads



6. QUALITY & RELIABILITY.

At STMicroelectronics before a new product and/or a technology can be introduced on the market it must pass several extensive reliability tests in order to meet ST internal stringent quality goals as well as most of the industry quality standards. PowerSO-10RF successfully passed the below reliability tests.

Table 2: Reliability Test Description

TEST	FEATURES	PURPOSE
H.T.B	Biased device at elevated temperature	To detect surface defects like poor passivism, contamination
T.H.B	Biased on in presence of steam	Metal corrosion detection
Thermal shock and thermal cycles.	Shock samples placed in liquids at high, low temperature. Cycles samples in high, low ambient temperature	Detect cracked die, wire bond breaking, and mechanical damage to package
Pressure pot & Pressure cooker.	High temperature & pressure with saturated steam	Electrochemical and galvanic corrosion
Marking permanency	10 strokes with brush per MIL standards	Measure resistance to solvent
Solderability	Verifies tinning process	Detect poor solder joints
Terminal ruggedness	Pull strength of the terminals	Detect poor welds

7. SOLDERING METHOD.

The key points which effect the reliability of a solder joint are obviously the choice of solder method, heat profile and solder paste. This matter has been subject to many publications and its detailed discussion is beyond the scope of this report. However, some guidelines are given here which may help the user in the choice of the appropriate soldering method.

Manufactures can generally choose between two methods of soldering: vapor phase soldering or infrared heating. Each has its own advantages but each creates thermal stresses in the devices. Before discussing the particular requirements of the PowerSO-10RF package a brief overview of the main principles of each method will be presented.

7.1 Vapor Phase Reflow.

Vapor phase reflow involves exposing the board to a per fluorocarbon vapor. The vapor condenses at the board surface on areas marked with a special fluorescent dye, and the latent heat evolved melts the solder. This provides stable heating in an oxygen-free atmosphere, a method which keeps the risk of damage to components low while guaranteeing reliable solder joints. The disadvantages of this technique are the high cost of the liquid and the effects of fluorocarbon gases on the environment.

7.2 Infrared Heating.

In infrared ovens, air or gas, such as nitrogen, is heated in a tunnel. Boards are carried through the heat on a conveyor belt. Components are heated through a combination of convection and radiation from the sources. The amount of heat applied to the board can be adjusted by controlling the heat of the source panels or lamps, the speed of the conveyor belt or the rate of circulation of the air or gas. This process cause much more thermal stress to the device than the previous one, as it heats the device completely, whereas vapor phase reflow applies heat only where it is required.

Both infrared and vapor phase reflow soldering techniques are appropriate for soldering the PowerSO-10RF. Infrared reflow soldering, however, is the most commonly used method.

7.3 Soldering Paste.

The choice of solder paste and the application of the right amount of paste in the correct shape are extremely critical for producing high yields in surface mounting. In order to reduce the time and heat required during the soldering process the alloys 63Sn/37Pb (melting point 187°C) or 62Sn/36Pb/2Ag (melting point 179°C) are preferred. These alloys are eutectic mixtures, which have a number of favorable characteristics:

- Fixed melting points at a low temperature;
- Pass directly from solid to liquid state;
- Solidify quickly.

7.4 Applying the Solder Paste.

Applying solder paste with a screening process is the most widely used technique. It is performed by aligning the board below the screen, by spreading the solder paste onto the screen and by moving a squeegee (a soft rubber tool) across it to push the paste through to the board at the appropriate points.

The screen itself consists of the screen mesh, the frame which holds the screen mesh aligned with the board and the mask. The screen mesh is designed to hold the solder paste in place until it is squeezed

through the mask by the squeegee. The screen mesh count refers to the number of openings per inch, which is selected according to the size of the solder particles in the paste used. For screen printing solder paste, the mesh count may vary from 60 to 150 and, in general, the size of the mesh opening should be chosen to be at least three times the size of the mean particle size in the solder paste. However, if the area of the openings is too large, there is a risk of the solder paste forming short-circuit bridges.

The distance between the PCB and the screen mesh is called the snap-on. When the squeegee passes over the screen, the mesh is stretched down to the board and then snapped back to this distance. The snap-off has to be set correctly to avoid the print being smeared. This parameter should be specified by the screen printer manufacturer and depends on the size of the board. The squeegee hardness and angle of attack also affect the results of the screen-printing. The screen and the squeegee should be restored frequently to obtain a good solder print on the board.

7.5 Placement of Parts and Drying.

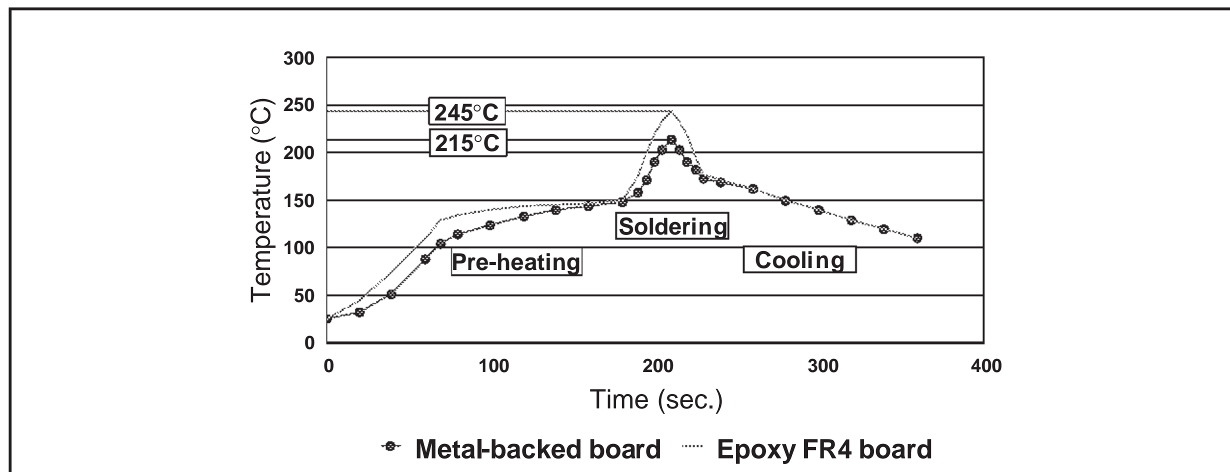
The surface mount components should be placed immediately after the solder past is applied to the PCB. Some misalignment is permitted, because the surface tension of the molten solder will align the PowerSO-10RF package with the pad layout of the board. The drying step follows after placement of the components is completed. The entire application should be baked in an oven for 45 min. at 50-80°C, to evaporate the moisture content of the solder paste and to minimize flux and solvent bubbling during the reflow solder process. This reduces the risk of voids, pinholes and poor wetting.

7.6 Avoiding Stresses.

There are two main stresses to the package during soldering:
- The first is due to high pressure caused by trapped moisture prior to soldering.
- The second is caused by different thermal expansion coefficient of the materials used in the package.

Usually the melting point of solder exceeds the maximum rating of the device, and so if the device is heated entirely to such temperatures, it may be damaged. Therefore, the thermal stress to which the devices are exposed must be minimized. This is generally achieved by using the appropriate solder heating profile. However, the correct soldering heat profile must be determined for each particular circuit by experiment.

Figure 7: Recommended Heat Profile / Reflow soldering



Stress caused by thermal shocks must be avoided by pre-heating the device to around 120-150°C. The temperature must then be increased to at least 30°C above the melting point of the selected solder paste and maintained long enough to allow a proper wetting and a homogeneous spread of the solder. However, in no circumstances should the device rating be exceeded. (Tpeak = 250°C for 10 sec.) In case of infrared heating, black surfaces (i.e. the plastic body of the package) absorb more heat than light-colored surfaces do (i.e. leads). The difference of temperature between case and leads should be less than 10°C. Once soldering is completed, device should not be forced cooled as it would induce mechanical stress and potential failure. Moreover as the thermal resistance of the solder joint is determined by the thickness of the applied solder, a thin layer of 2-4mils, after reflow, is recommended.

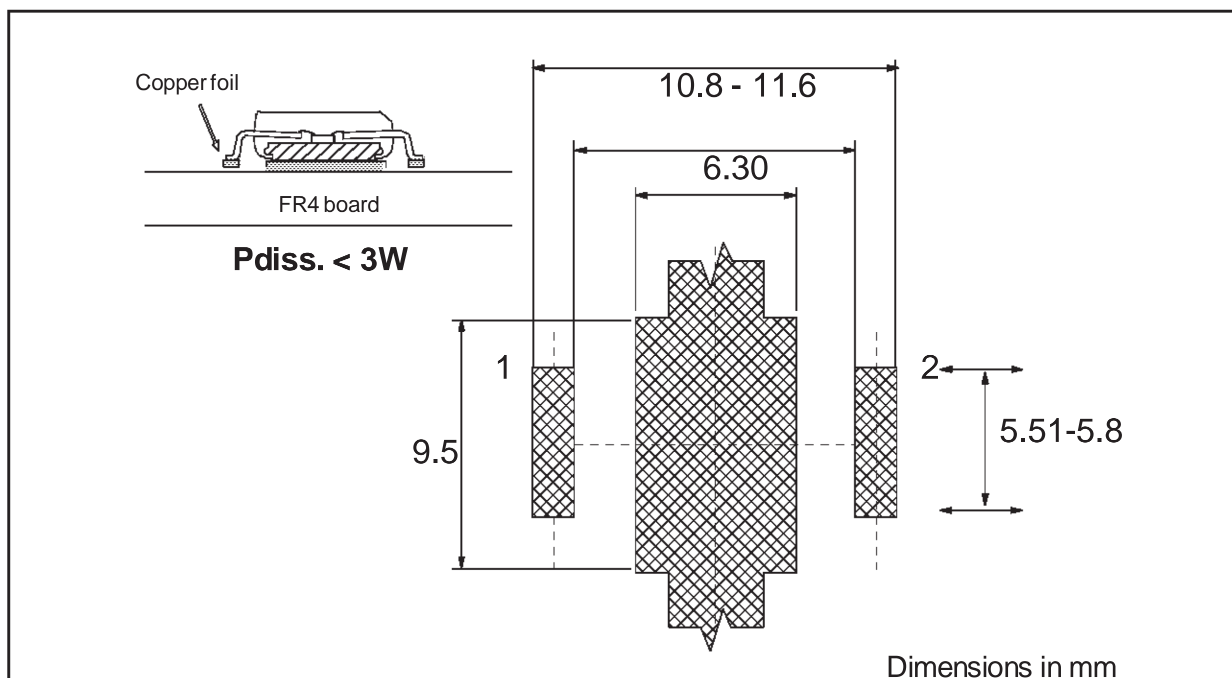
8. MOUNTING RECOMMENDATIONS.

Epoxy-glass PCBs are commonly used as mounting substrate for electronic applications. However, their poor conductivity (approximately 50°C/W) make them poorly suited to surface mount power applications. However some existing techniques can be applied to improve thermal performance considerably.

The simplest way is to design a layout with copper area of suitable dimension on the board, and use this area as a heat spreader. Measurements have been made using a 1.6mm (60 mils) thick FR4 board with a copper layer of 35 microns. The copper area was varied from 3 to 10cm^2. The thermal resistance was decreased to 25°C/W for a 6cm on-board-heatsink.

The maximum power dissipation capability is between 2W and 3W.

Figure 8: PowerSO-10RF recommended pad layout



To allow higher power dissipation capability on a conventional epoxy-glass PCB, copper-filled through holes sited under the slug can be used.

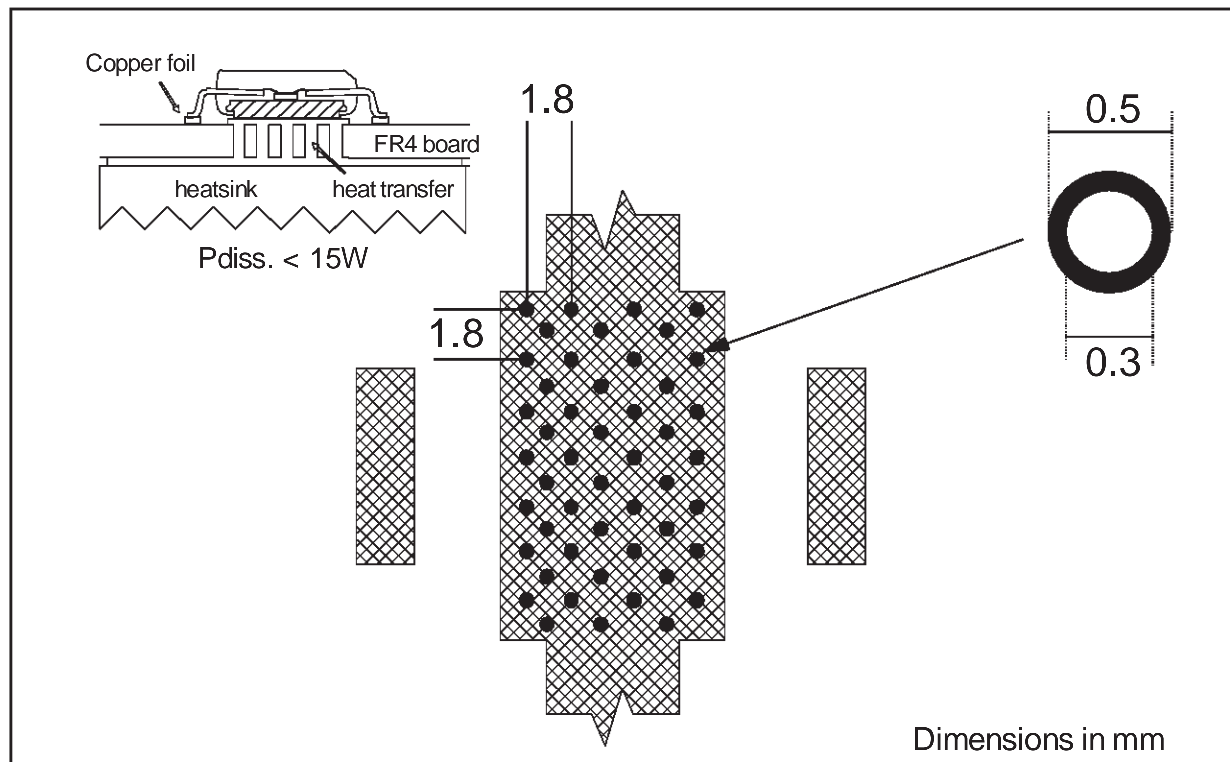
Several experiments were carried out with PowerSO-10RF formed-leads and the summary is as follows:

A. FR4 PCB - 1.6 mm (60 mils) thick
49 holes with a pitch of 1.8 mm and an internal diameter of 0.3 mm
PCB thermal resistance < 3.5°C/W

B. FR4 PCB - 0.5 mm (20 mils) thick
49 holes with a pitch of 1.8 mm and an internal diameter of 0.3 mm
PCB thermal resistance < 2.5°C/W

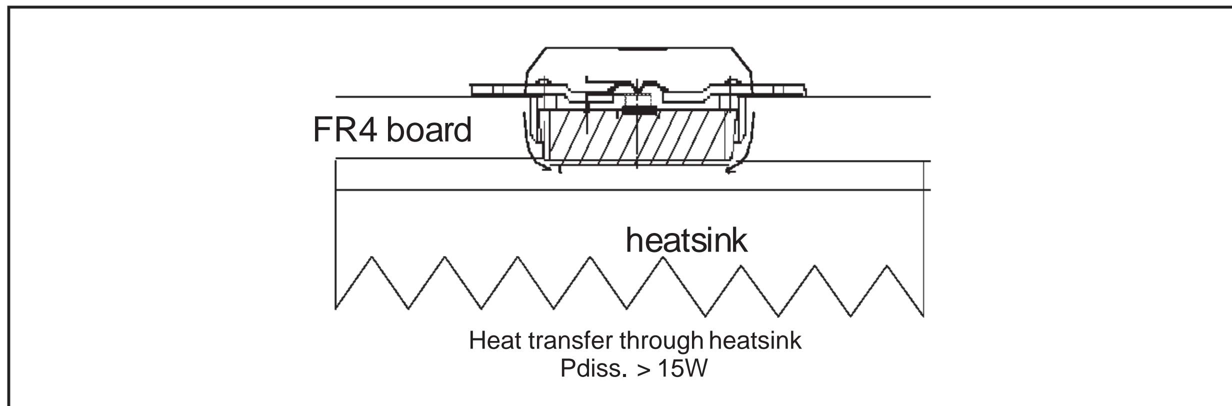
The maximum power dissipation capability is between 15W and 20W.

Figure 9: PowerSO-10RF recommended pad layout with via holes



A more sophisticated solution is the use of a metal backed board consisting on a copper (or Cu alloy) base plate glued with the PCB. By using this type of board, the RF LDMOS device in PowerSO-10RF straight-leads package can be soldered directly to the copper layer. Thus the heat generated by this device is directly transferred to the base plate and as a result the overall thermal resistance is significantly reduced. In this case, the PowerSO-10RF device and the external heatsink that can be connected to the copper base plate only limit the maximum power dissipation capability. So this solution can be used for all applications where the power dissipation is higher than 15W.

Figure 10: Mounting on copper base plate



9. THERMAL RESISTANCE AND MAXIMUM POWER DISSIPATION CAPABILITY.

The table below gives the thermal resistance and the maximum allowed power dissipation for the LDMOS PD5xxxx family in PowerSO-10RF plastic package under different mounting configurations:

- **Mounting 1:** 1.6 mm FR4-PCB / 6 cm copper area beneath PowerSO-10RF. PCB-RTH < 25°C/W
- **Mounting 2:** 1.6mm FR4-PCB / 49 holes (1.8 mm pitch / 0.3 mm internal diameter) connected on heatsink. PCB-RTH < 3.5°C/W
- **Mounting 3:** 0.5 mm FR4-PCB / same configuration than Mounting 2. PCB-RTH < 2.5°C/W
- **On heatsink:** PowerSO-10RF soldered directly on heatsink.

Note: Calculations are made considering a maximum junction temperature of 165°C and a heatsink temperature of 70°C.

Table 3: Thermal resistance and maximum power dissipation

Part number	RTHj-slug (max)	Max Pdiss. On heatsink	Max Pdiss. Mounting 1	Max Pdiss. Mounting 2	Max Pdiss. Mounting 3
PD54003 (S)	1.8°C/W	52.8W	3.5W	17.9W	22.1W
PD54008 (S)	1.3°C/W	73.1W	3.6W	19.8W	25.0W
PD55003 (S)	3.0°C/W	31.7W	3.4W	14.6W	17.3W
PD55008 (S)	1.8°C/W	52.8W	3.5W	17.9W	22.1W
PD55015 (S)	1.3°C/W	73.1W	3.6W	19.8W	25.0W
PD57002 (S)	20°C/W	4.75W	2.1W	4.0W	4.2W
PD57006 (S)	5.0°C/W	19.0W	3.2W	11.2W	12.7W
PD57018 (S)	3.0°C/W	31.7W	3.4W	14.6W	17.3W
PD57030 (S)	1.8°C/W	52.8W	3.5W	17.9W	22.1W
PD57045 (S)	1.3°C/W	73.1W	3.6W	19.8W	25.0W

Note: By adding the suffix (S) means PowerSO-10RF straight-leads version

10. CONCLUSION

The need for RF surface mount packages with high power capability will increase dramatically as surface mount technology becomes even more widespread. Power surface mount packages that can house even larger die and have lower thermal resistances will become popular. PowerSO-10RF, the RF optimized version of PowerSO-10 first ST JEDEC approved, is the best solution and is the next step in STMicroelectronics long-term strategy to reduce component cost and improve manufacturability for applications up to 2.5GHz.

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